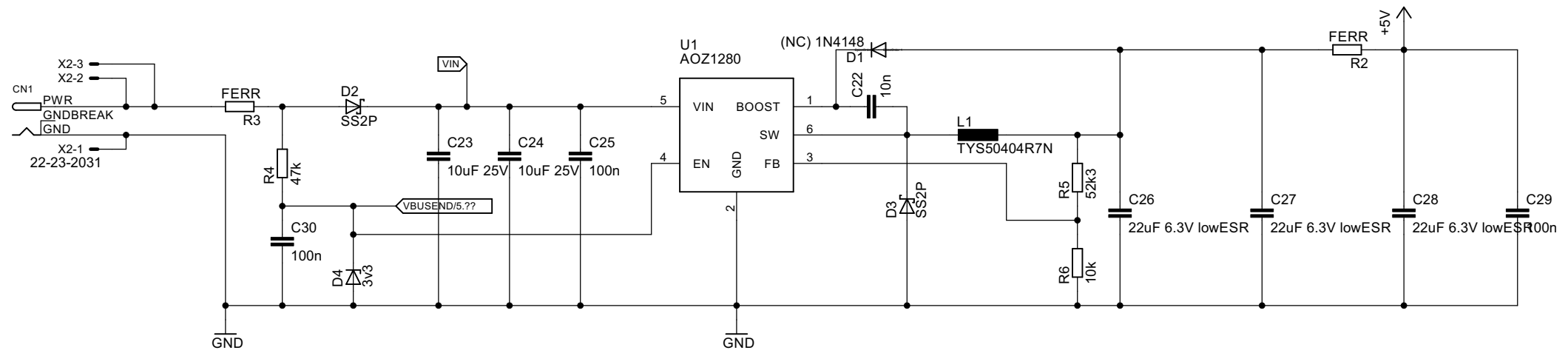
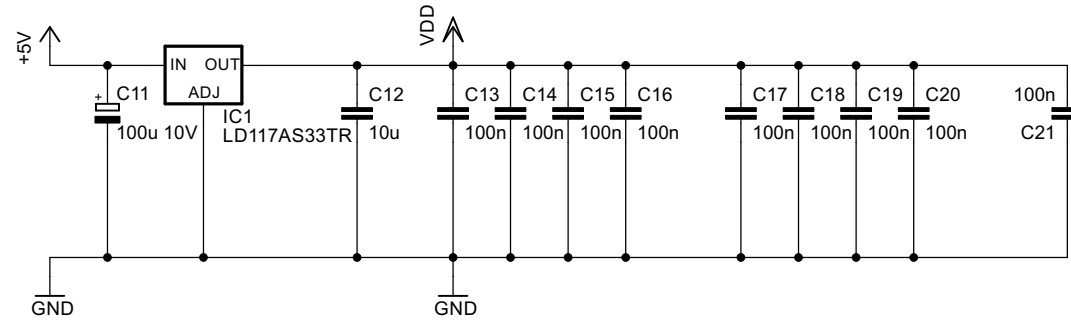
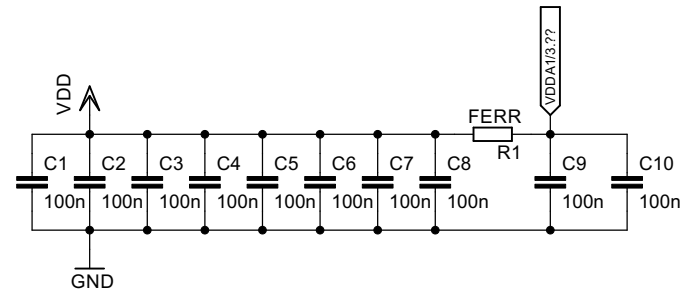
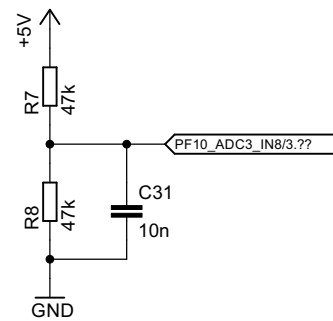


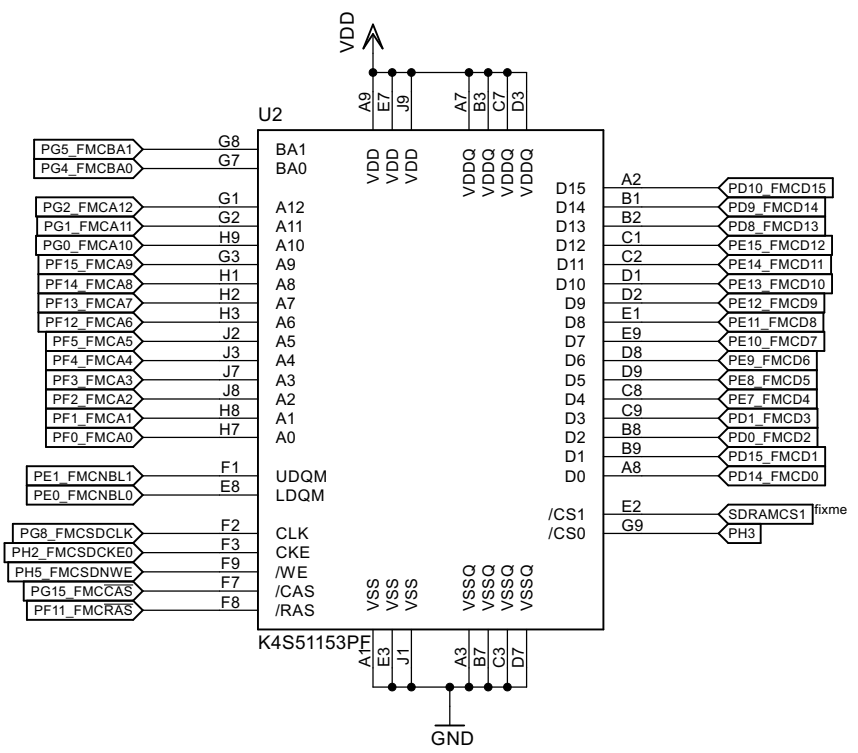
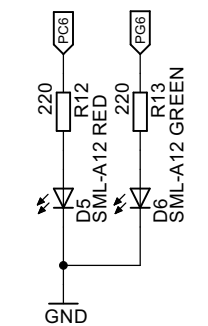
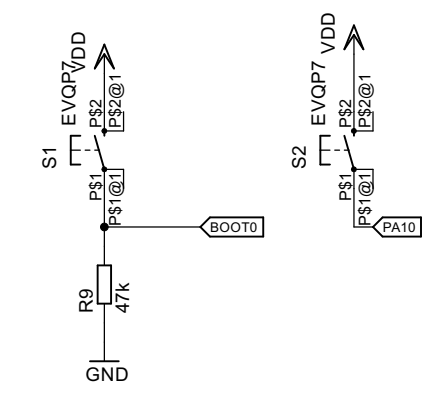
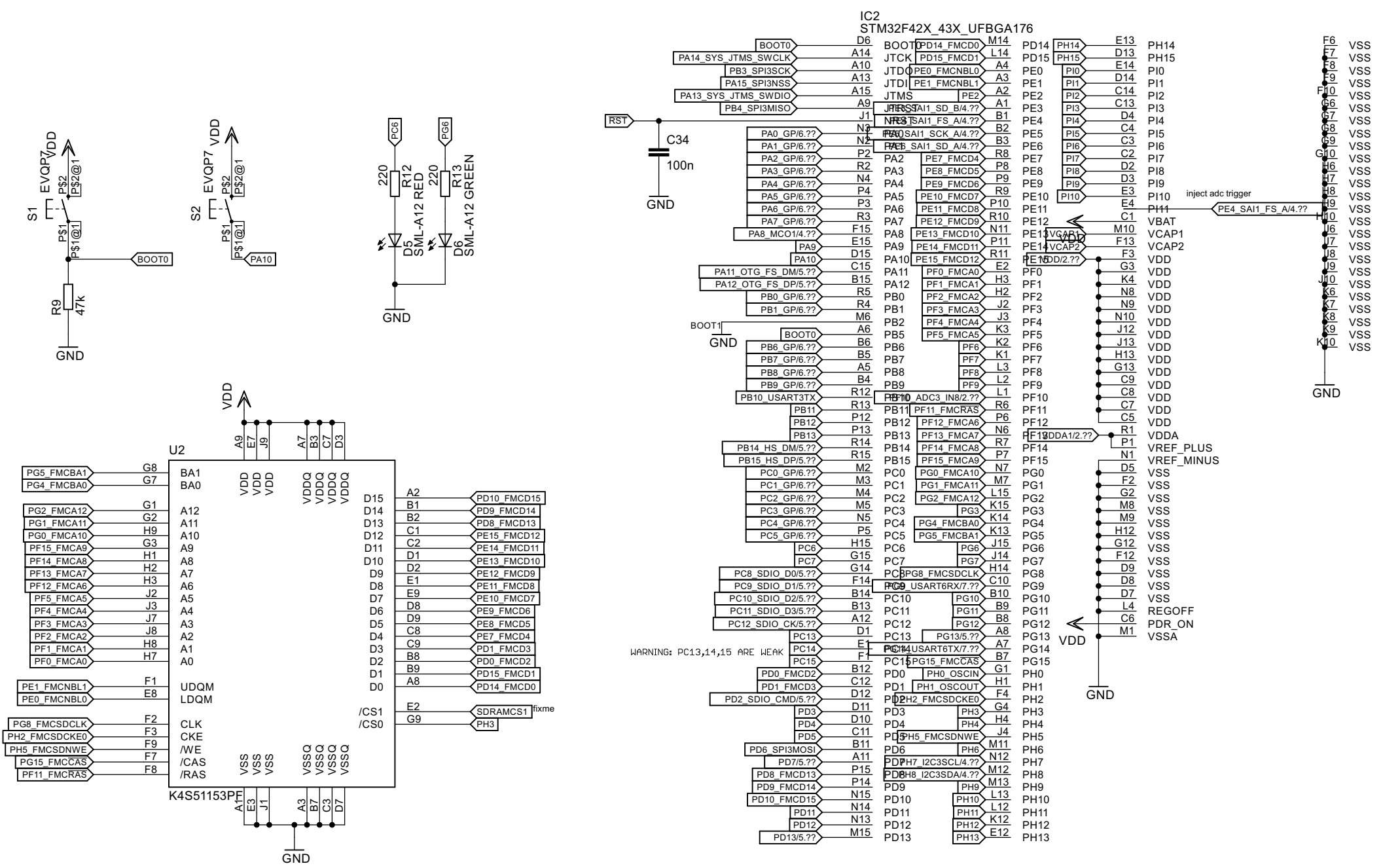
# Axoloti Core 1.2 Schematics

by Johannes Taelman

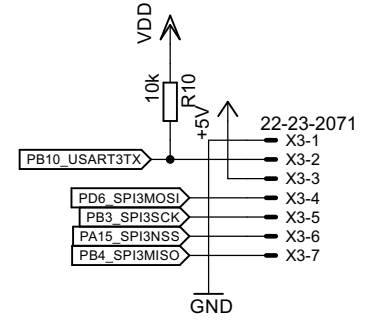


5V voltage supervisor

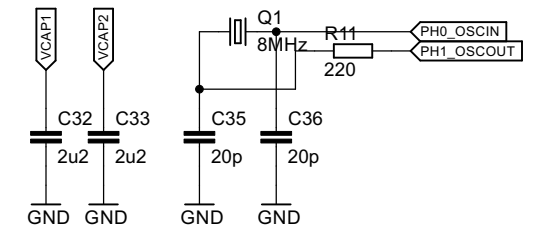
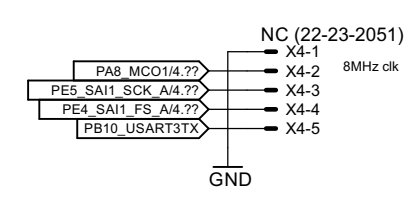




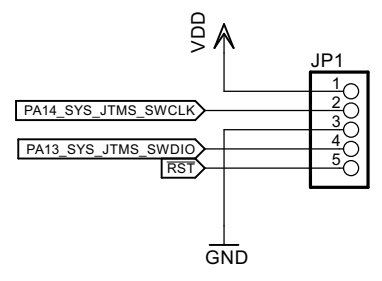
Multiprocessor stream

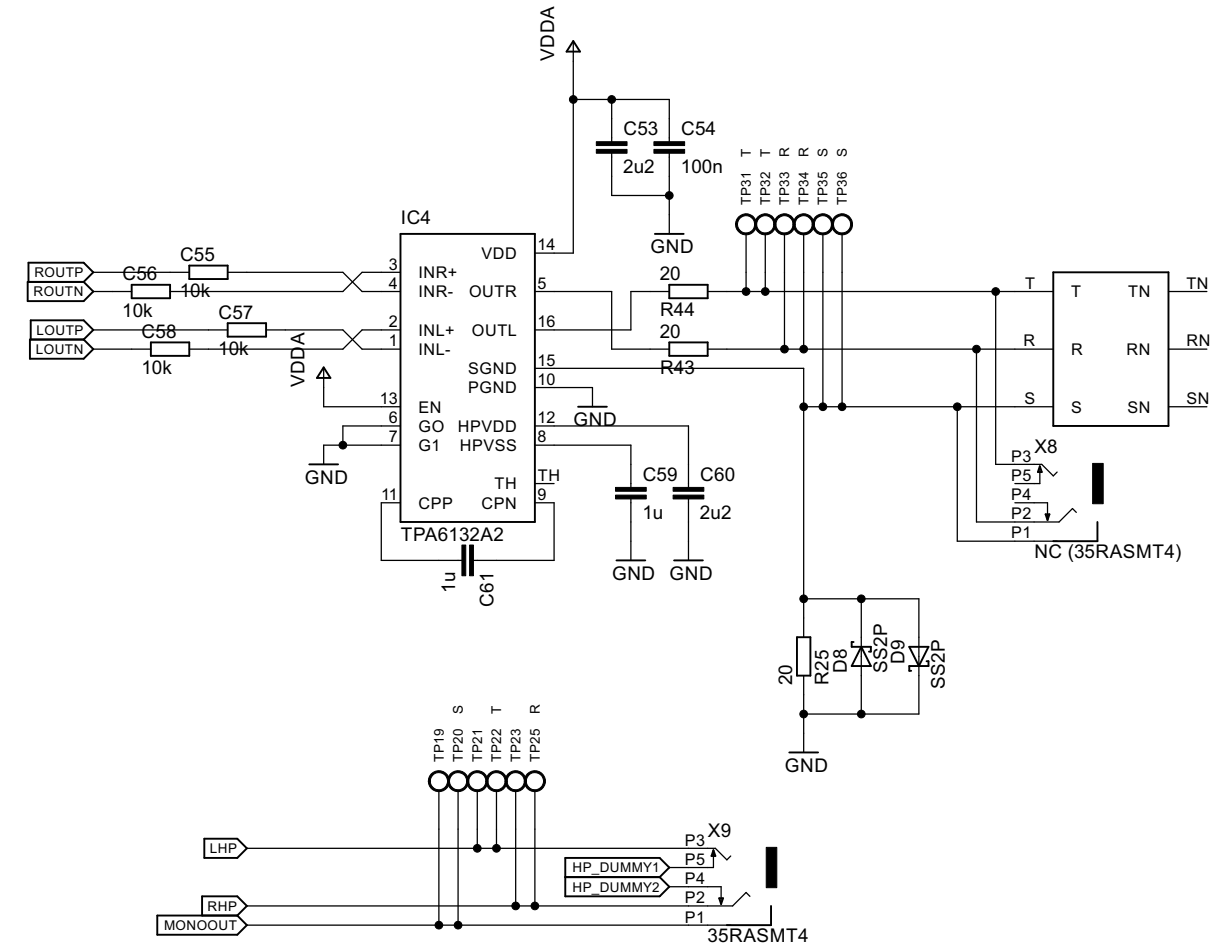
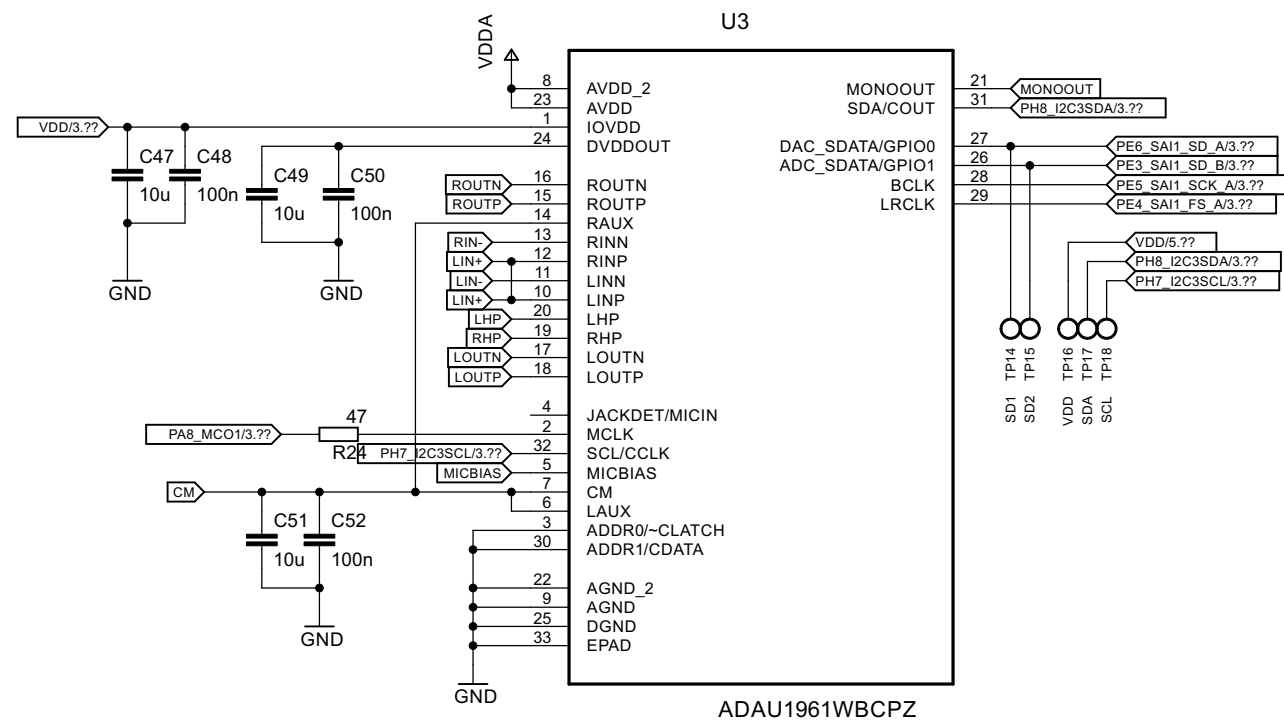
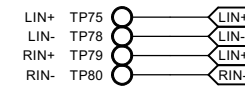
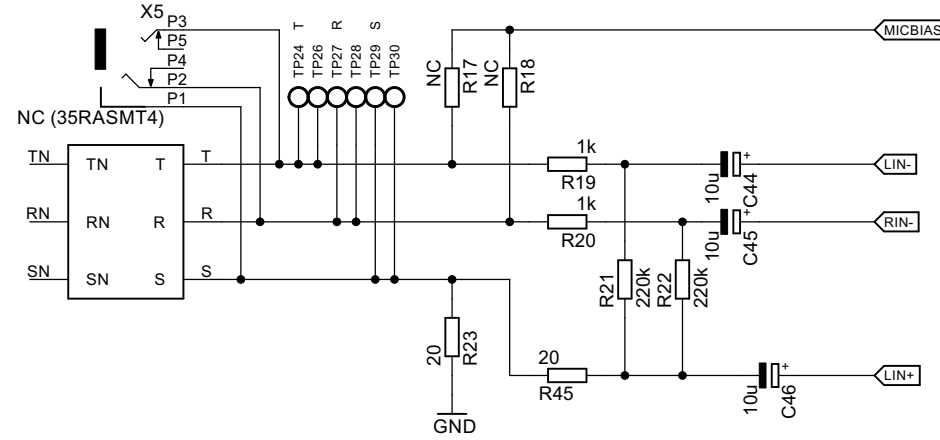
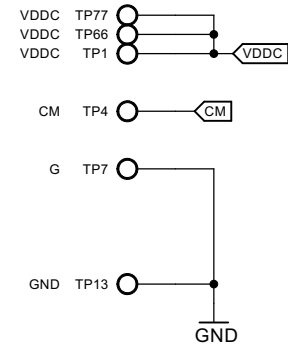
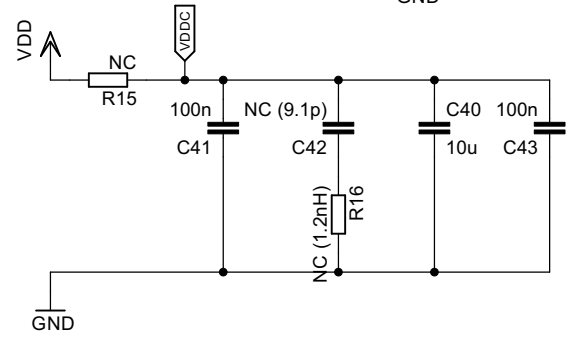
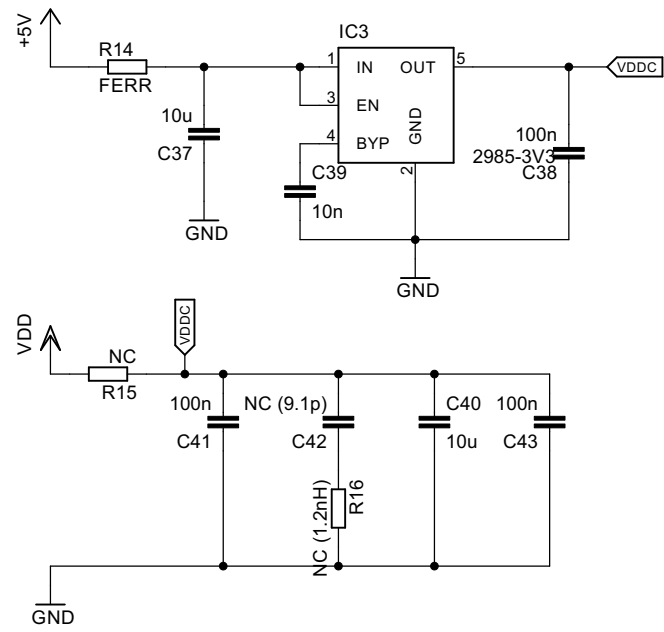


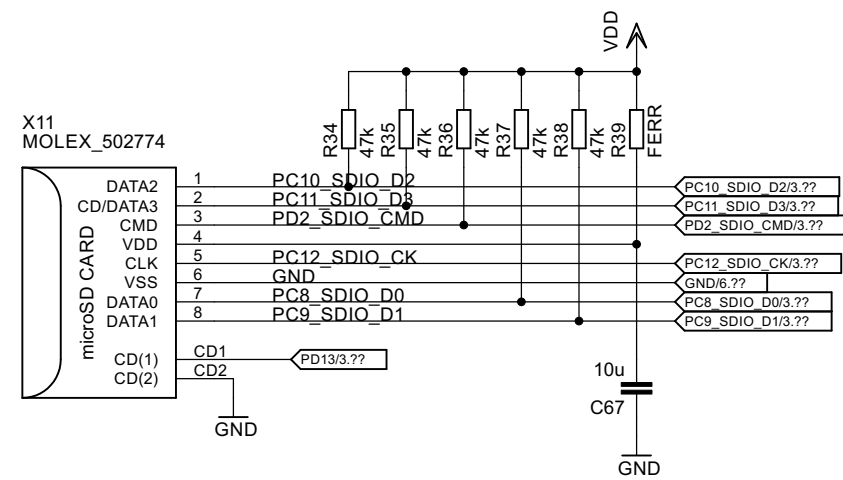
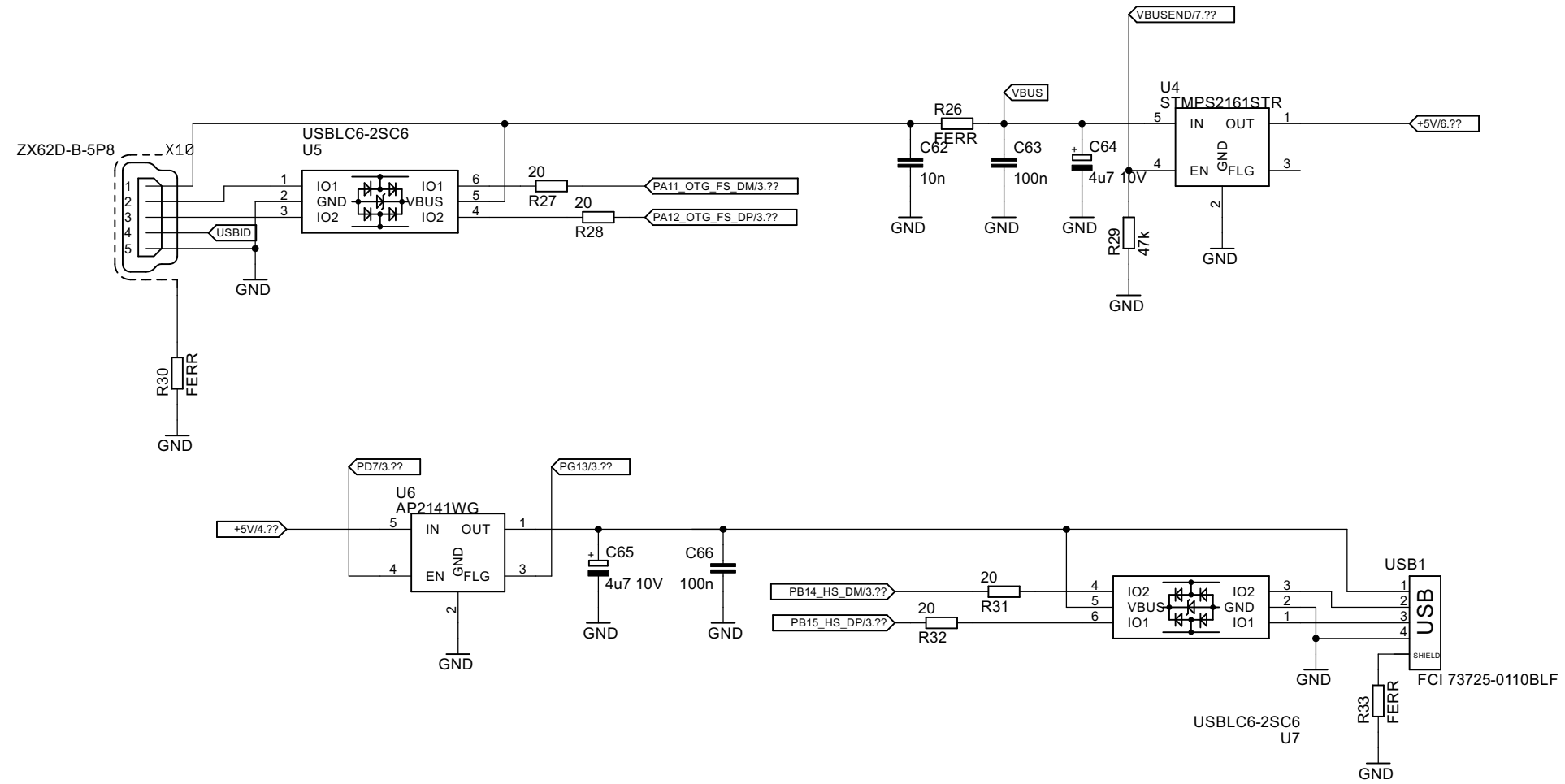
Multiprocessor sync

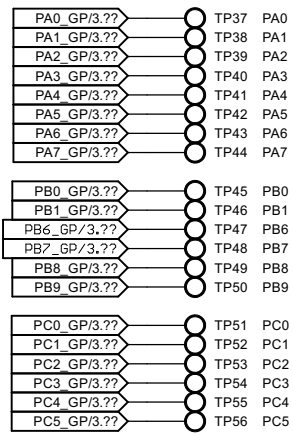


SWD









	ADC	DAC	SPI	I2C	UART
PA0	ADC1_IN0				
PA1	ADC1_IN1				
PA2	ADC1_IN2				TX
PA3	ADC1_IN3				RX
PA4	ADC1_IN4	DAC_OUT1	NSS		
PA5	ADC1_IN5	DAC_OUT2	SCK		
PA6	ADC1_IN6		MISO		
PA7	ADC1_IN7		MOSI		
PB0	ADC1_IN8				
PB1	ADC1_IN9				
PB6					
PB7					
PB8				I2C1_SCL	
PB9				I2C1_SDA	
PC0	ADC1_IN10				
PC1	ADC1_IN11				
PC2	ADC1_IN12				
PC3	ADC1_IN13				
PC4	ADC1_IN14				
PC5	ADC1_IN15				

